

**Constraining Designs For Synthesis And
Timing Analysis: A Practical Guide To
Synopsys Design Constraints (SDC)**

By Sanjay Churiwala



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Qiuyang Wu has been in the EDA industry for 15 years, with expertise in STA, Synthesis, Timing Constraints: Are they constraining designs or designers? http://www.tauworkshop.com/2015/slides/Sripada_Panel_TAU_15_PPT.pptx

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To understand this evolution it is important to understand the life cycle of a design constraint. first do logic synthesis, then do placement,
http://en.wikipedia.org/wiki/Design_constraint

This paper presents Timing Characterization and constraining Tool After the successful physical synthesis, the design was checked against functional correctness
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